A structure-driven performance analysis of sparse matrix-vector multiplication

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Outline

Introduction

2 Experimental Design

- 3 Research Questions : Effect of Matrix Structure
 - On the Choice of Storage Format
 - Within a Storage Format
 - Along with Hardware Characteristics

4 Summary and Future Work

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Background : Sparse Matrix Storage Formats

COO :

0

0

2

6 2 7 3 5

1 1

3 2

row 0

col

val

- A sparse matrix : a matrix in which most of the elements are zero.
- Basic sparse storage formats :
 - Coordinate Format (COO)
 - Compressed Sparse Row Format (CSR)
 - Diagonal Format (DIA)
 - ELLPACK Format (ELL)



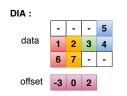
2 3 3

0

3

CSR :





ELL :

data

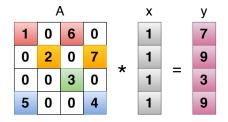


indices	0	1	2	0
	2	3	-	3

Background : SpMV

Sparse Matrix-Vector Multiplication

- y = Ax, where A is a sparse matrix and the input vector x and output vector y are dense.
- Working set size : sizeof(A) + sizeof(x) + sizeof(y)



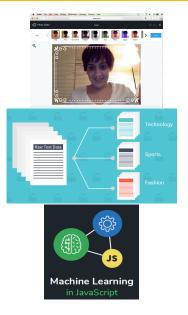
• Web-enabled devices everywhere!

- Various compute-intensive applications involving sparse matrices on the web.
 - Image editing
 - Computer-aided design
 - Text classification (data mining)
 - Deep learning
- Recent addition of WebAssembly to the world of JavaScript.



Why Sparse Matrices on the Web?

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Apply data and low-level code optimizations to a single format.

Depends on the structure of the matrix and the machine characteristics.

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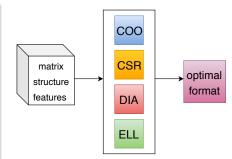
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To understand the effect of :

- matrix structure on the choice of storage format.
- matrix structure on the SpMV performance within a storage format.
- interaction between matrix structure and hardware characteristics on the SpMV performance.



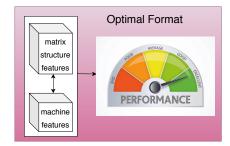
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Developed a reference set of sequential C and hand-tuned WebAssembly implementations of SpMV for different formats on same algorithmic lines.

```
void spmv_coo(int *row, int *col, float *val, int nnz, int N, float *x, float *y)
{ int i;
  for(i = 0; i < nnz ; i++)
     y[row[i]] += val[i] * x[col[i]];
}</pre>
```

Listing 1: Single-precision SpMV COO implementation in C

- **Benchmarks** : Around 2000 real-life sparse matrices from The SuiteSparse Matrix Collection.
- Sparse Storage Formats : COO, CSR, DIA, ELL
- Measured SpMV Performance for C and WebAssembly in FLOPS (Floating point operations per second).

• Machine Architecture

Intel Core i7-3930K with 6 3.20GHz cores, 12MB last-level cache and 16GB memory,running Ubuntu Linux 16.04.2

• C

Compiled with gcc version 7.2.0 at optimization level -O3

• WebAssembly

Used Chrome 74 browser (Official build 74.0.3729.108 with V8 JavaScript engine 7.4.288.25) as the execution environment with –experimental-wasm-simd flag to enable the use of SIMD instructions.

x%-affinity

We say that an input matrix A has an x%-affinity for storage format F, if the performance for F is at least x% better than all other formats and the performance difference is greater than the measurement error.

Example

For example, if input array A in format CSR, is more than 10% faster than input A in all other formats, and 10% is more than the measurement error, then we say that A has a 10%-affinity for CSR.

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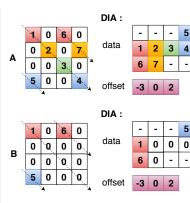


Research Questions : Effect of Matrix Structure • On the Choice of Storage Format

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- dia_ratio = $\frac{ndiag_elems}{nnz}$ where, nnz : number of non-zeros, ndiag_elems : number of elements in the diagonals
- Indicates if the given matrix is a good fit for DIA format or not.
- dia_ratio(A) = 7/7 = 1
- dia_ratio(B) = 7/3 = 2.33

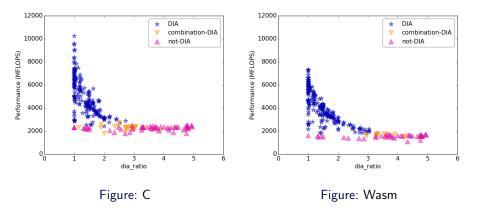


4

-

DIA Format

Matrices with dia_ratio $\leq =$ 3 show affinity towards the DIA format, except for a few matrices.



Relationship between Storage Format and Structure Features

Format	It Feature(s)	
DIA	$dia_ratio \leq 3$ and large N	1
ELL	ell_ratio $\simeq 1$ and small max_nnz_per_row	2
C00	nnz < N or small <i>avg_nnz_per_row</i> and uneven number of non-zeros per row	3

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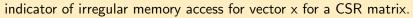
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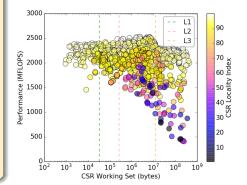


SpMV Performance within CSR Matrices

- CSR Working Set : (N+1) + 2*nnz + 2*N
- Irregular access for vector x affects performance.
- Introduced some new matrix structure features : *ELL Locality Index, CSR Locality Index*
- Based on data locality model
- Using reuse-distance concept



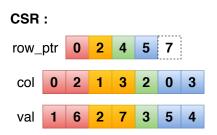




CSR Locality Index : Step 1

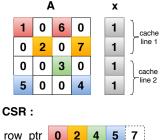
- Calculate Row Reuse Distance for each non-zero.
- Row Reuse Distance (rrd) : Distance from the last non-zero whose column index corresponds to the same cache line of the input vector x.
- Unit of distance : rows
- *Assume the cache line size to be 2 and cache size to be fixed for this example.

A	1	0	6	0
	0	2	0	7
	0	0	3	0
	5	0	0	4



CSR Locality Index : Step 1

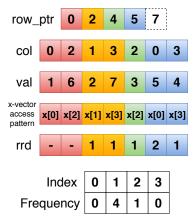
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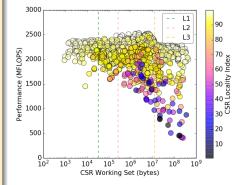
- Calculate CSR Reuse Distance using frequency distribution over Row Reuse Distance (rrd).
- CSR Reuse Distance[p] : the number of non-zeros of sparse matrix A stored in the CSR format which access the input vector x with p Row Reuse Distance.

CSR :



CSR Locality Index : Step 3

- Calculate CSR Locality Index using cumulative percentage over CSR Reuse Distance.
- CSR Locality Index = $\frac{\sum_{p=0}^{15} CSR Reuse Distance[p]}{nnz} \times 100$
- This feature accounts for :
 - spatial locality for the non-zeros in a row.
 - temporal locality for the non-zeros in the neighbouring rows.
- * We chose the limit to be 15 based on our experiments



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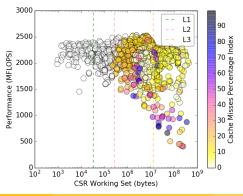
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Cache Memory : CSR Performance

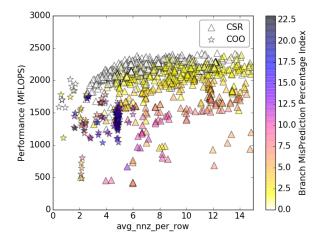
- Features based on data locality model have their roots in the hardware features like data cache misses.
- Measured true performance counters using PAPI tool.

• Index =
$$\frac{PAPI_L1_DCM\lor PAPI_L2_DCM\lor PAPI_L3_TCM}{nnz}$$
 × 100



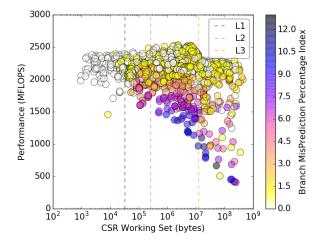
Branch Prediction Unit : CSR vs COO

• Index = $\frac{PAPI_BR_MSP}{PAPI_BR_PRC+PAPI_BR_MSP} \times 100$



Branch Prediction Unit : CSR Performance

• Index = $\frac{PAPI_BR_MSP}{PAPI_BR_PRC+PAPI_BR_MSP} \times 100$



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- The optimal choice of storage format is governed both by the structure of the matrix and the code optimization opportunities available.
- Due to different code generation strategy, the SpMV performance suffers in the case of WebAssembly for Chrome (v8) browser.
- Our data locality based structure features estimate if the SpMV performance is affected by the irregular memory accesses for vector x.
- We validate our evaluations and parameter choices using hardware performance counters.

Future Work

- Further explore to quantify the impact of additional hardware features on SpMV performance via matrix structure features.
- Explore new optimization opportunities for hand-tuned WebAssembly implementations through the upcoming WebAssembly instructions.
- Develop parallel versions of SpMV based on multithreading features like web workers.
- Develop automatic techniques to choose the best format for web-based SpMV.

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